Nanocatlyst Fabrication Using a Stencil Mask

Jeremy Robinson

Materials Science and Engineering

University of California – Berkeley

Advisor: Oscar Dubon

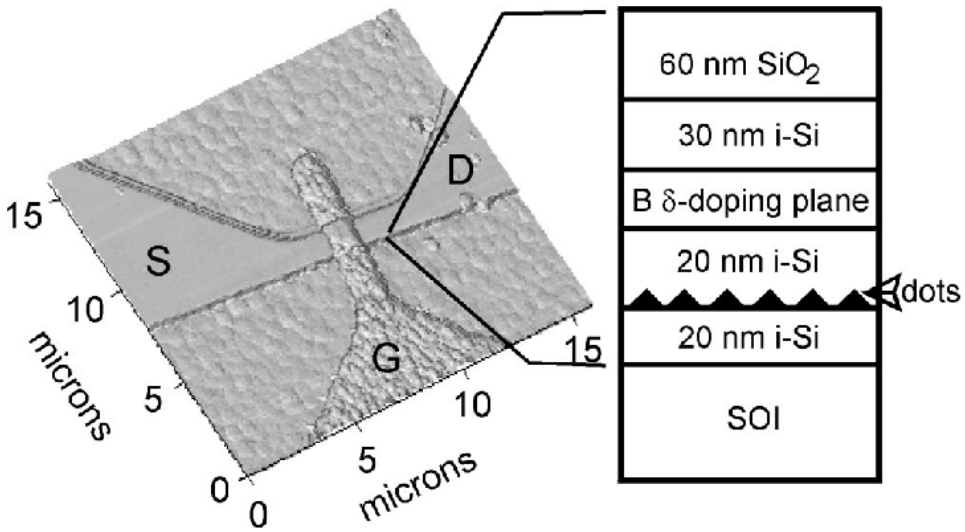
Materials Science and Engineering

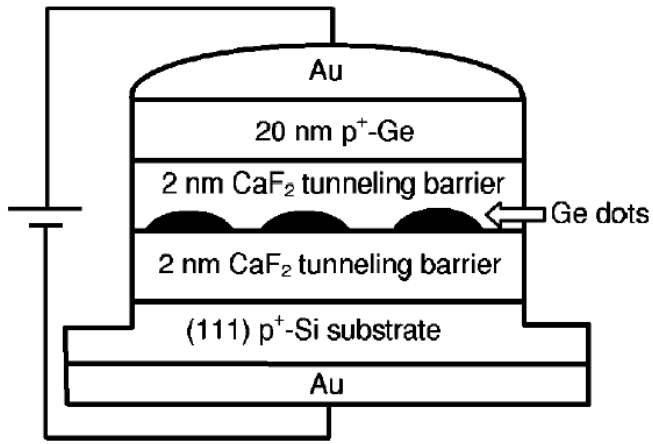
Outline

1. Introduction and Background
2. Vapor-Liquid-Solid Growth Mechanism
3. Nanofabrication Procedure
   a. Stencil Mask Design
   b. Exposures and Etching
4. Summary

Introduction

Quantum Dots for MOS-FETs and resonant tunneling diodes





GeÕSi quantum-dot metal–oxide–semiconductor field-effect transistor, Appl. Phys. Lett. **81**, A. I. Yakimov, A. V. Dvurechenskii, V. V. Kirienko, and A. I. Nikiforov

Growth and characterization of CaF2 Õ GeÕ CaF2 Õ Si — 111 – quantum dots for resonant tunneling diodes operating at room temperature, Appl. Phys. Lett. **80**, A. I. Yakimov, A. S. Derjabin, et al.

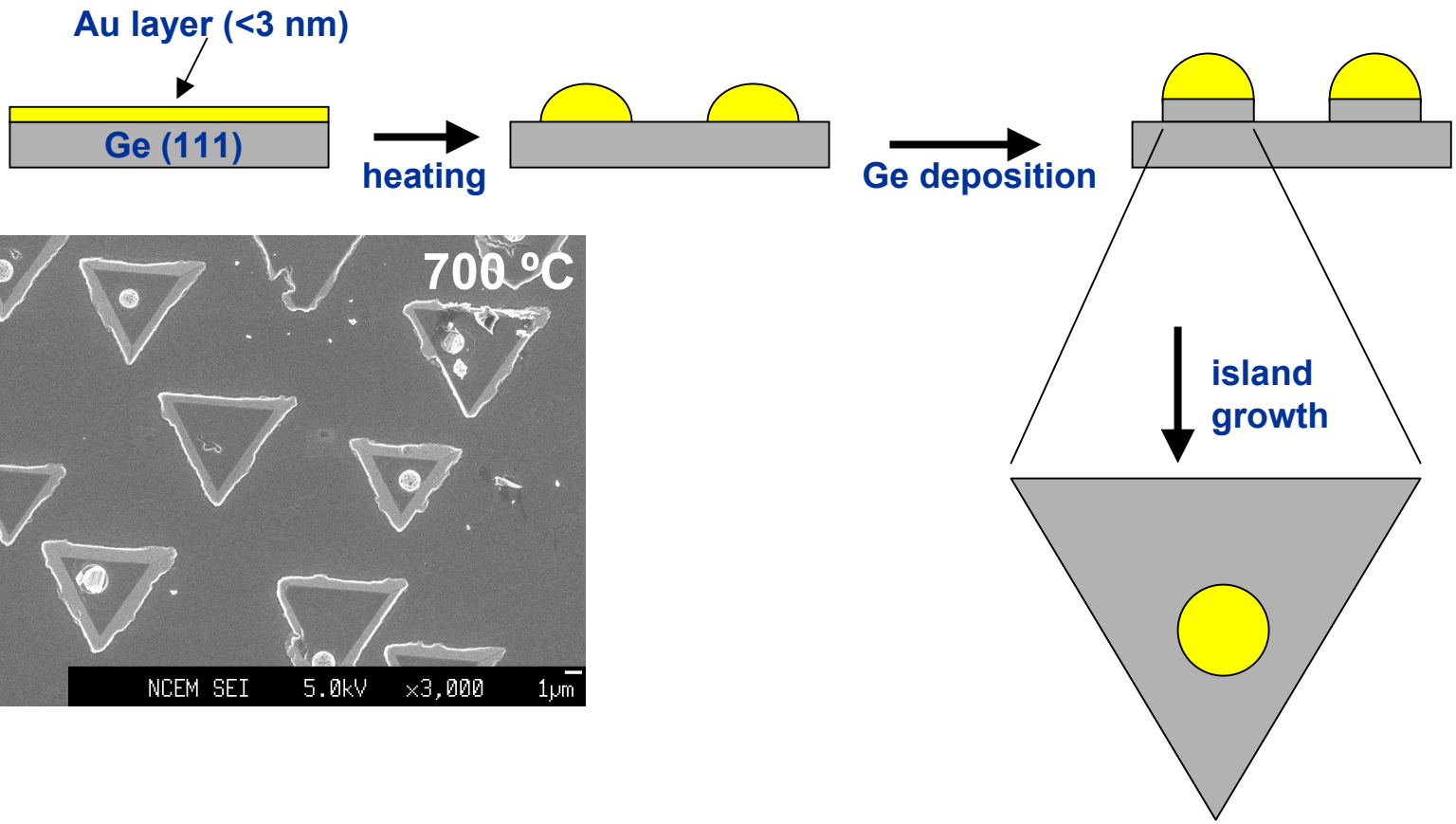
Vapor-liquid-solid synthesis of Ge islands

Increase the number of growth parameters to control the size, density and arrangement of grown semiconductor islands

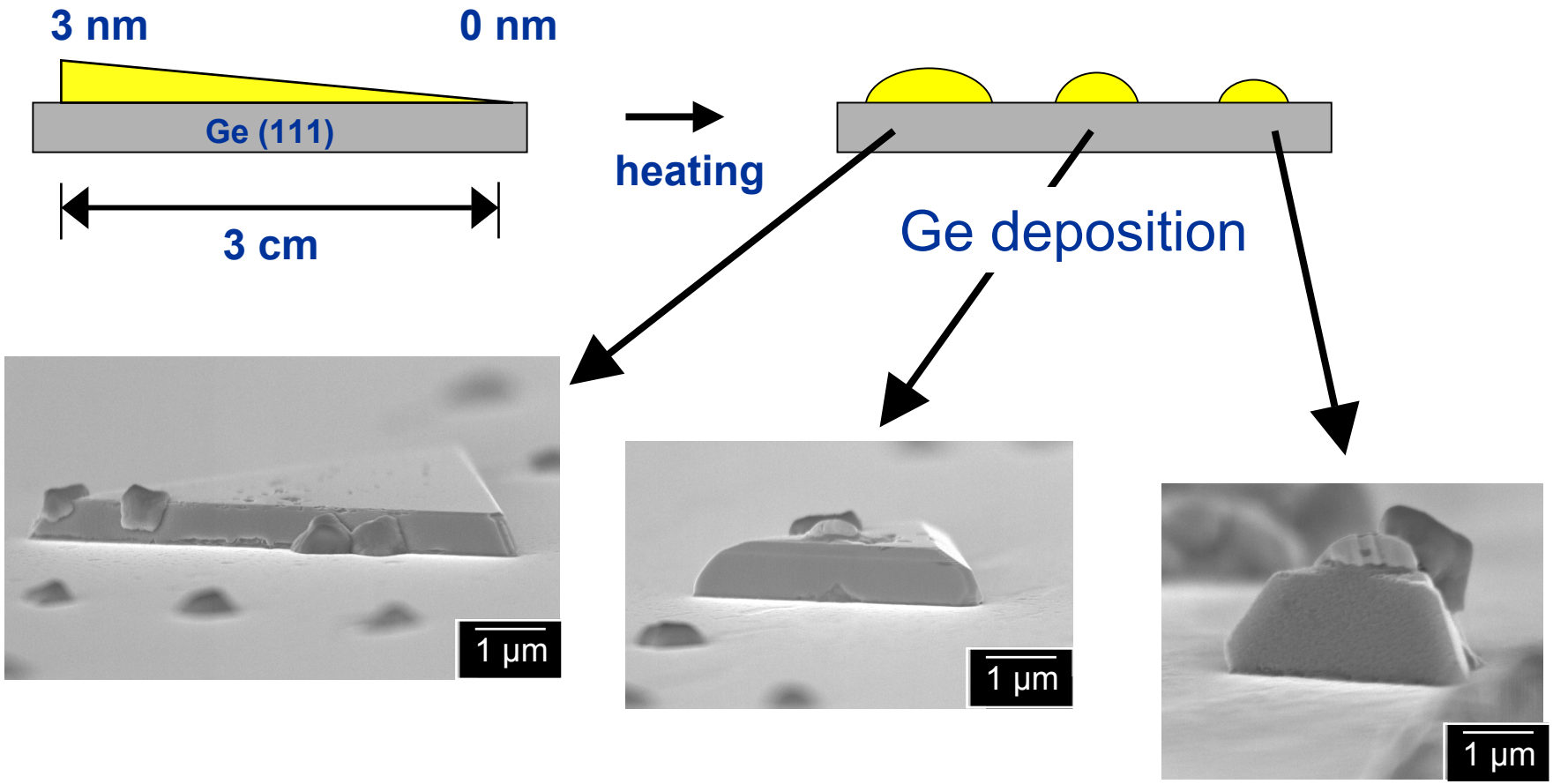
Droplet-induced island nucleation and growth by a vapor-liquid-solid approach

Ge island synthesis

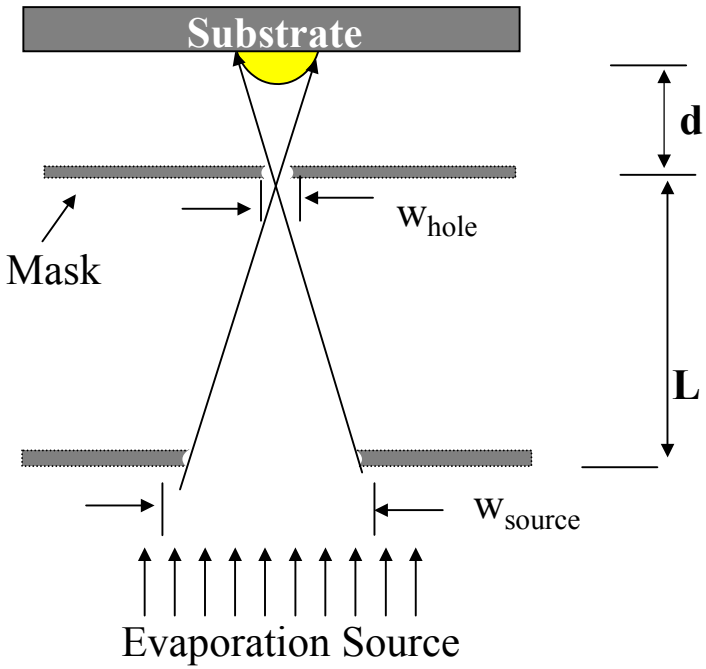
- Island nucleation on Ge (111) at Au-Ge eutectic droplets
- Solid-source molecular beam epitaxy

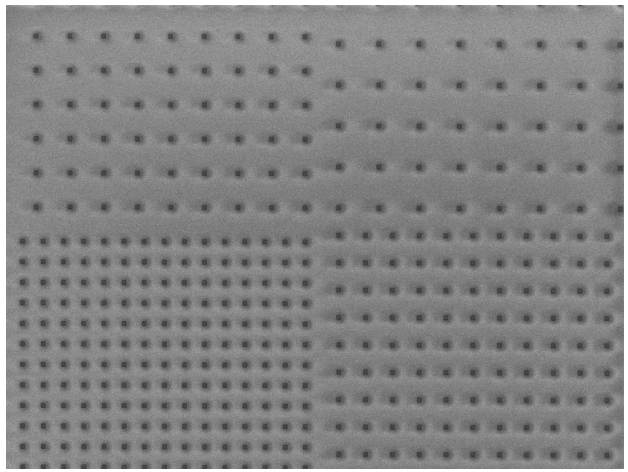


Island Size Versus Au Layer Thickness

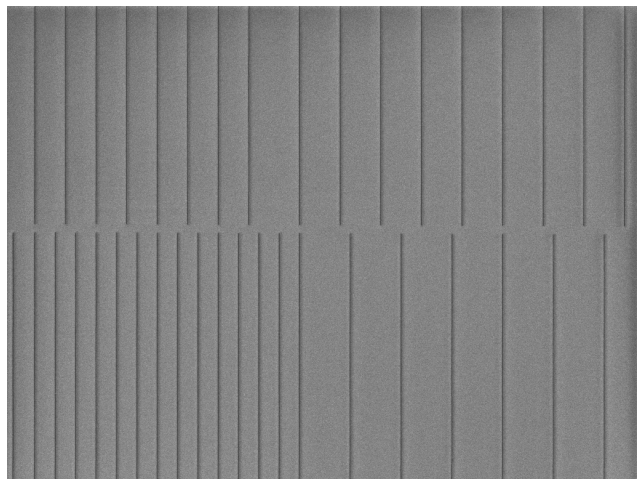


Stencil Mask Design





Features: 25nm – 300nm



$$w_{dot} \approx w_{hole} + \left(\frac{d}{L}\right) w_{source}$$

Wafer Processing

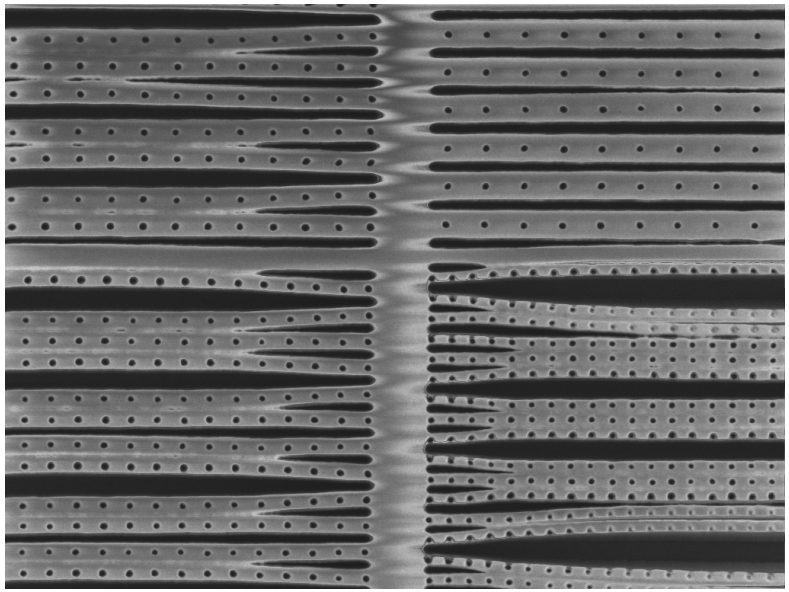
Wafer Database

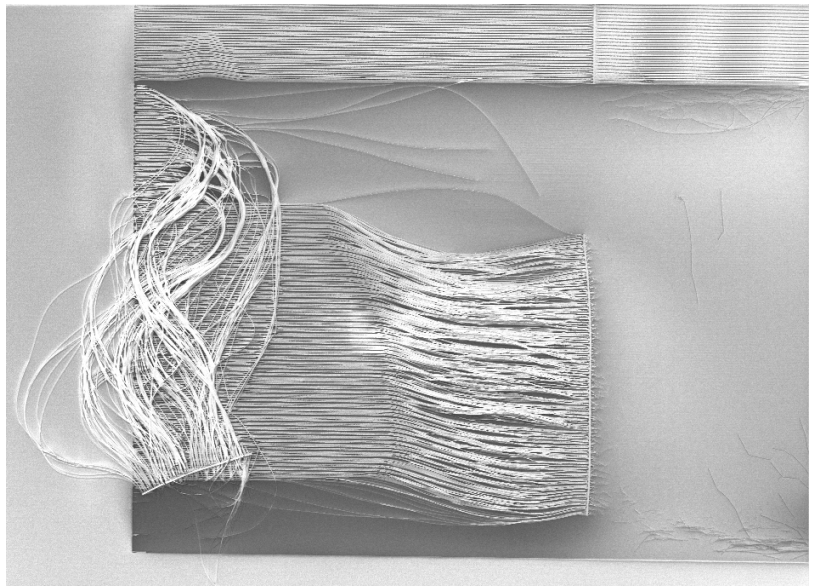
1900	Wafer ID
Fri., May. 9, 2003	Started (date)
Fri., May. 9, 2003	Deactivated (date: mm/dd/yyyy)
Bruce	Operator
UCBerkeley	Customer
	Instruction sheet

Ge Au catalysed nucleation and growth experiment

1. Spin 11.6% KRS-XE @ 1000 rpm
2. PAB 110 C, 3mins
3. Expose with GEISLES3, 75 uC/cm2
4. Develop LDD26W 75s
5. O2 descum 20s
6. Nitride etch

1st Exposure

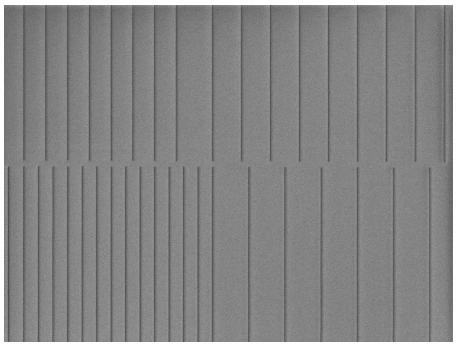
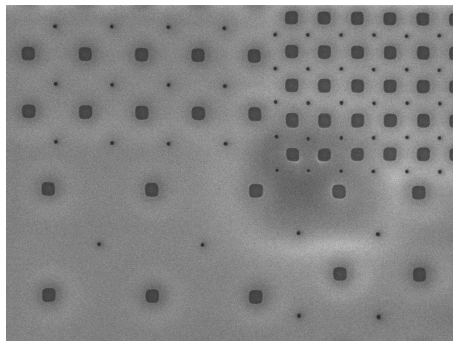
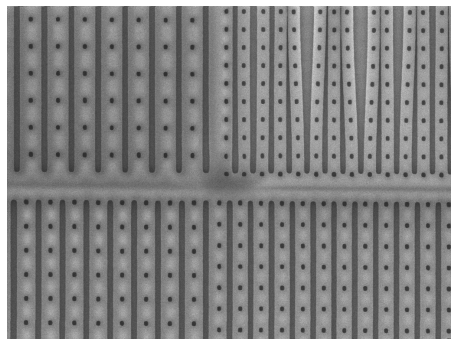




- Line spacings were too close
- Upper end of dose range was too large

2nd Exposure

- Examples of the final patterned features for the SiN windows.

- Etch rates for SiN and developed KRS

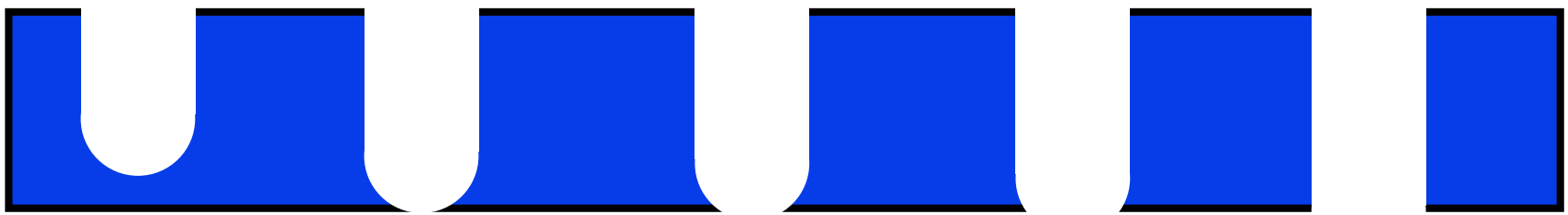
	Etch Rate: SiN	Etch Rate: KRS
CHF_4/O_2	~80A/min	~90A/min
SF_6 (large features)	~350A/min	~300A/min
SF_6 (small features)	>500A/min	~300A/min

Membrane Exposure

- Exposed and Developed SiN membranes

- We expect the size to be small than the patterened feature

- An Isotropic etch will make a bowl shaped feature in the membrane



Summary

- We have designed a variety of features to be patterened on SiN membrane windows.
- We have begun a process that can produce stencil mask features smaller than the patterened features.
- The etch mask will be used for paterning metal features on Ge and Si wafers.
- The resulting evaporated structures wuill be used in a VLS process to study the equilibrium shape evolution of Ge islands.

Acknowledgements

Thanks to Alex Liddle, Weilun Chao, and Erik Anderson